

INFORMAZIONI PERSONALI

Guido Masera

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Sesso maschile | Data di nascita 05/09/1962 | Nazionalità Italiana

INCARICO PER IL QUALE SI CONCORRE:

ESPERTO NELLA VALUTAZIONE DI PIANI DI SVILUPPO (L.R.14/2011) E DI PROGETTI DI RICERCA (L.R. 84/1993)

POSIZIONE RICOPERTA:

PROFESSORE ASSOCIATO IN INGEGNERIA ELETTRONICA PRESSO IL POLITECNICO DI TORINO

TITOLO DI STUDIO

LAUREA IN INGEGNERIA ELETTRONICA E DOTTORATO DI RICERCA

ESPERIENZA
PROFESSIONALE

dal 01/02/1987 al 30/10/1988

dal 01/01/1991 al 30/06/1995

dal 01/07/1995 al 01/11/1998

dal 01/11/1998 a oggi

Ricercatore presso presso CSELT (ora Telecom Italia Lab), Torino

Collaboratore tecnico presso il Dipartimento di Elettronica del Politecnico di Torino

Ricercatore universitario presso il Politecnico di Torino

Professore II fascia presso il Politecnico di TORINO

ISTRUZIONE E FORMAZIONE

Ottobre 1990

13/10/1986

Luglio 1981

Dottore di Ricerca – Politecnico di Torino

Laurea in Ingegneria Elettronica – Politecnico di Torino

Diploma di maturità classica – Liceo Balbo, Chieri

COMPETENZE PERSONALI

Lingua madre Italiano

Altre lingue

	COMPRENSIONE		PARLATO		PRODUZIONE SCRITTA
	Ascolto	Lettura	Interazione	Produzione orale	
Inglese	Livello avanzato	Livello avanzato	Livello avanzato	Livello avanzato	Livello avanzato
Francese	Livello intermedio	Livello intermedio	Livello base	Livello base	Inserire il livello

Competenze professionali
specifiche nella valutazione

- Valutazione di progetti internazionali di ricerca per conto di:
 - Swiss National Science Foundation (<http://www.snf.ch/en/Pages/default.aspx>) (1 progetto valutato nel 2013)
 - Agence National Recherche (Francia, <http://www.agence-nationale-recherche.fr/>) (3 progetti valutati nel 2010, 2012 e 2014)
 - Agency for Innovation by Science and Technology, Belgio (<http://www.iwt.be/>) (1 progetto valutato nel 2008)
 - Georgian National Science Foundation (Georgia) (3 progetti valutati nel 2011 e 2013) (https://www.zsi.at/de/object/partner/1863?_wrapper=print)
 - MINISTERO DELL'ISTRUZIONE, DELL'UNIVERSITÀ E DELLA RICERCA (2 progetti FIRB valutati nel 2011)
 - Università di Pisa (1 progetto valutato nel 2007)
 - Comune di Milano (1 progetto valutato nel 2006)
- Referente del Dipartimento di Elettronica e Telecomunicazioni del Politecnico di Torino per la valutazione della qualità della didattica e della ricerca e per la compilazione delle schede SUA dei corsi di studio e dei dipartimenti (www.anvur.org/)
- Membro della Commissione paritetica per la didattica del Politecnico di Torino (<http://www.cpd.polito.it/>)

ULTERIORI INFORMAZIONI

Pubblicazioni Si vede elenco allegato

ALLEGATI

- Elenco delle pubblicazioni scientifiche negli ultimi 5 anni

Torino, 18/5/2015

G. L. Nero

**ALLEGATO: ELENCO DELLE PUBBLICAZIONI DEL PROF. GUIDO MASERA
NEGLI ULTIMI 5 ANNI**

(18 maggio 2015)

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Author Name

- ☐ Masera, G. (42)
- ☐ Martina, M. (21)
- ☐ Condo, C. (11)
- ☐ Awais, M. (8)
- ☐ Baghdadi, A. (5)

Subject Area

- ☐ Engineering (32)
- ☐ Computer Science (28)
- ☐ Mathematics (6)
- ☐ Physics and Astronomy (3)
- ☐ Biochemistry Genetics and Molecular Biology (1)

Document Type

- ☐ Article (26)
- ☐ Conference Paper (15)
- ☐ Editorial (1)

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Reducing the Dissipated Energy in Multi-standard Turbo and LDPC Decoders

Condo, C., Baghdadi, A., Masera, G. 2015 Circuits, Systems, and Signal Processing 0

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Parallel H.264/AVC fast rate-distortion optimized motion estimation by using a graphics processing unit and dedicated hardware

Shahid, M.U., Ahmed, A., Martina, M., Masera, G., Magli, E. 2015 IEEE Transactions on Circuits and Systems for Video Technology 0

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A joint source/channel approach to strengthen embedded programmable devices against flash memory errors

Martina, M., Condo, C., Masera, G., Zamboni, M. 2014 IEEE Embedded Systems Letters 0

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A parallel radix-sort-based VLSI architecture for finding the first W Maximum/Minimum Values

Xiao, G., Martina, M., Masera, G., Piccinini, G. 2014 IEEE Transactions on Circuits and Systems II: Express Briefs 0

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Unified turbo/LDPC code decoder architecture for deep-space communications

Condo, C., Masera, G. 2014 IEEE Transactions on Aerospace and Electronic Systems 0

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VLSI implementation of a non-binary decoder based on the analog digital belief propagation

Awais, M., Masera, G., Martina, M., Montorsi, G. 2014 IEEE Transactions on Signal Processing 0

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Simplified log-MAP algorithm for very low-complexity turbo decoder hardware architectures

Martina, M., Papaharalabos, S., Mathiopoulos, P.T., Masera, G. 2014 IEEE Transactions on Instrumentation and Measurement 2

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Molecular transistor circuits: From device model to circuit simulation

Zahir, A., Zaidi, S.A.A., Pulimeno, A., (...), Masera, G., Piccinini, G. 2014 Proceedings of the 2014 IEEE/ACM International Symposium on Nanoscale Architectures, NANOARCH 2014 0

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Rediscovering logarithmic diameter topologies for low latency network-on-chip-based applications

Condo, C., Martina, M., Roch, M.R., Masera, G. 2014 Proceedings - 2014 22nd Euromicro International Conference on Parallel, Distributed, and Network-Based Processing, PDP 2014 0

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A novel decoder architecture for error resilient JPEG2000 applications based on MQ arithmetic

Zeza, S., Masera, G., Nooshabadi, S. 2014 Proceedings - IEEE International Symposium on Circuits and Systems 0

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Variable parallelism cyclic redundancy check circuit for 3GPP-LTE/LTE-advanced

Condo, C., Martina, M., Piccinini, G., Masera, G. 2014 IEEE Signal Processing Letters 0

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Energy-efficient multi-standard early stopping criterion for low-density-parity-check iterative decoding

Condo, C., Baghdadi, A., Masera, G. 2014 IET Communications 0

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A joint communication and application simulator for NoC-based custom SoCs: LDPC and turbo codes parallel decoding case study

Condo, C., Baghdadi, A., Masera, G. 2013 Proceedings - 16th Euromicro Conference on Digital System Design, DSD 2013 1

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VLSI architecture for low-complexity motion estimation in H.264 multiview video coding

Ahmed, A., Usman Shahid, M., Martina, M., Magli, E., Masera, G. 2013 Proceedings - 16th Euromicro Conference on Digital System Design, DSD 2013 0

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FPGA accelerator of quasi cyclic EG-LDPC codes decoder for NAND flash memories

Zaidi, S.A.A., Awais, M., Condo, C., Martina, M., Masera, G. 2013 Conference on Design and Architectures for Signal and Image Processing, DASIP 0

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19	Analysis on parallel implementations of fixed-complexity sphere decoder	Wu, B., Masera, G.	2013	Science China Information Sciences	0
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20	VLSI implementation of a multi-mode turbo/LDPC decoder architecture	Condo, C., Martina, M., Masera, G.	2013	IEEE Transactions on Circuits and Systems I: Regular Papers	15
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21	Power control for crossbar-based input-queued switches	Bianco, A., Giaccone, P., Masera, G., Ricca, M.	2013	IEEE Transactions on Computers	3
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22	A 2.63 Mbit/s VLSI implementation of SISO arithmetic decoders for high performance joint source channel codes	Zeza, S., Nooshabadi, S., Masera, G.	2013	IEEE Transactions on Circuits and Systems I: Regular Papers	3
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23	Reducing the memory for iteration-exchanged information and border future metrics in the HomePlug AV turbo decoder implementation	Guerrieri, L., Bisaglia, P., Martina, M., Masera, G.	2012	International Symposium on Turbo Codes and Iterative Information Processing, ISTC	0
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24	FFT implementation using QCA	Awais, M., Vacca, M., Graziano, M., Masera, G.	2012	2012 19th IEEE International Conference on Electronics, Circuits, and Systems, ICECS 2012	6
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25	Flexible radio design: Trends and challenges in digital baseband implementation	Masera, G., Baghdadi, A., Kienle, F., Moy, C.	2012	VLSI Design	3
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26	Efficient VLSI implementation of soft-input soft-output fixed-complexity sphere decoder	Wu, B., Masera, G.	2012	IET Communications	5
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27	A Network-on-Chip-based turbo/LDPC decoder architecture	Condo, C., Martina, M., Masera, G.	2012	Proceedings -Design, Automation and Test in Europe, DATE	8
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28	A system view on iterative MIMO detection: Dynamic sphere detection versus fixed effort list detection	Gimmler-Dumont, C., Kienle, F., Wu, B., Masera, G.	2012	VLSI Design	6
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29	An application specific instruction set processor based implementation for signal detection in multiple antenna systems	Tamagnone, M., Martina, M., Masera, G.	2012	Microprocessors and Microsystems	3
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30	Non-recursive max * operator with reduced implementation complexity for turbo decoding	Papaharalabos, S., Mathiopoulos, P.T., Masera, G., Martina, M.	2012	IET Communications	7
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31	On practical implementation and generalizations of max * Operator for turbo and LDPC decoders	Martina, M., Masera, G., Papaharalabos, S., Mathiopoulos, P.T., Gioulekas, F.	2012	IEEE Transactions on Instrumentation and Measurement	9
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32	An LDPC decoder architecture for wireless sensor network applications	Brioli, A.D.G., Martina, M., Masera, G.	2012	Sensors	3
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33	High speed architectures for finding the first two maximum/minimum values	Amarù, L.G., Martina, M., Masera, G.	2012	IEEE Transactions on Very Large Scale Integration (VLSI) Systems	11
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34	A high throughput turbo decoder VLSI architecture for 3GPP LTE standard	Ahmed, A., Awais, M., Rehman, A.U., Maurizio, M., Masera, G.	2011	Proceedings of the 14th IEEE International Multitopic Conference 2011, INMIC 2011	4
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35	A flexible NoC-based LDPC code decoder implementation and bandwidth reduction methods	Condo, C., Masera, G.	2011	Conference on Design and Architectures for Signal and Image Processing, DASIP	1
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36	VLSI implementation of 16-point DCT for H.265/HEVC using walsh hadamard transform and lifting scheme	Ahmed, A., Awais, M., Maurizio, M., Masera, G.	2011	Proceedings of the 14th IEEE International Multitopic Conference 2011, INMIC 2011	5
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☐ 37	A novel architecture for scalable, high throughput, multi-standard LDPC decoder	Awais, M., Singh, A., Boutillon, E., Masera, G.	2011	Proceedings - 2011 14th Euromicro Conference on Digital System Design: Architectures, Methods and Tools, DSD 2011	4
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☐ 38	Scalable, high throughput LDPC decoder for WIMAX (802.16e) applications	Awais, M., Singh, A., Masera, G.	2011	Communications in Computer and Information Science	3
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☐ 42	State metric compression techniques for turbo decoder architectures	Martina, M., Masera, G.	2011	IEEE Transactions on Circuits and Systems t: Regular Papers	11
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					Top of page

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