INFORMAZIONI PERSONALI

Andrea L. LACAITA

Via F. Dall'Ongaro, 5, 20133, Milano (Italy)
+39.02.7610962 +39.3317610962
andrea.lacaita@libero.it
http://www.deib.polimi.it/ita/personale/dettagli/234110

Sesso M | Data di nascita 20/02/1962 | Nazionalità Italiana

POSIZIONI RICOPERTE

2000 - oggi — **Politecnico di Milano**

Professore Ordinario di Elettronica

Oggi titolare degli insegnamenti di "Dispositivi elettronici " e "Analog Circuit Design", Facoltà di Ingegneria Industriale e dell'Informazione.
Coordina il Laboratorio di Micro e Nanoelettronica del Dipartimento di Elettronica, Informazione e Bioingegneria

1992 – 2000 — **Politecnico di Milano**

Titolare di insegnamenti di Tecnologie Elettroniche, Elettronica Applicata, Elettronica II, Optoelettronica, Elettronica dello Stato Solido.
Fonda e coordina il Laboratorio di Micro e Nanoelettronica del Dipartimento di Elettronica e Informazione

1987- 1992 — **Consiglio Nazionale delle Ricerche**

Ricercatore presso il Centro di Elettronica Quantistica e Strumentazione Elettronica. Milano

ISTRUZIONE E FORMAZIONE

1980 – 1985 — **Laurea In Ingegeneria Nucleare**

Politecnico di Milano

ALTRE ESPERIENZE PROFESSIONALI

2002- oggi — Valutatore e revisore di progetti di ricerca finanziati.

2011 — Academic Visitor - Data Storage Institute, Singapore

1999 — Visiting Scientist - IBM T.J. Watson Research Center, Yorktown Heights, NY

1989-90 — Visiting Scientist - AT&T Bell Labs, Murray Hill

Ruoli organizzativi gestionali

2013-oggi: Direttore PoliFAB – Infrastruttura di Ateneo per le Micro e Nanotecnologie
2011-oggi : Consigliere di Amministrazione Fondazione Politecnico
2007-2008: Componente del Senato Accademico del Politecnico di Milano
2006-08: Direttore del Dipartimento di Elettronica e Informazione del Politecnico di Milano

COMPETENZE PERSONALI

Lingua madre: Italiano

Inglese

COMPRENSIONE		PARLATO		PRODUZIONE SCRITTA
C1	C1	C1	C1	C1

Competenze comunicative: Ottime competenze comunicative acquisite durante la mia esperienza di docente e ricercatore

Competenze professionali: Progettazione di sistemi e componenti elettronici . Tecnologie elettroniche e microelettroniche

ULTERIORI INFORMAZIONI

Pubblicazioni: E' coautore di oltre 350 lavori scientifici di cui circa 200 pubblicati in riviste internazionali e di numerose relazioni invitate

Appartenenza a gruppi / associazioni: Dal 2015 è Presidente dell'Associazione Gruppo Italiano di Elettronica – coordinamento accademico dei professori unversitari e ricercatori di elettronica italiani
2014 - eletto Socio corrispondente residente dell'Istituto Lombardo Accademia di Scienze e Lettere.
2009 - nominato IEEE Fellow "for contributions to advances of single-photon detectors and non-volatile memories" e Distinguished Lecturer

Dati personali: Autorizzo il trattamento dei miei dati personali ai sensi del Decreto Legislativo 30 giugno 2003, n. 196 "Codice in materia di protezione dei dati personali".

Prof. Andrea Leonardo LACAITA, Elenco Pubblicazioni 2010-15

Articoli in Rivista

- G. M. Paolucci, C. Monzio Compagnoni, A. S. Spinelli, A. L. Lacaita, A. Goda: *Fitting cells into a narrow VT interval: physical constraints along the lifetime of an extremely scaled NAND Flash memory array.* IEEE Transactions on Electron Devices (ISSN:0018-9383), pp. 1491-1497, 62 (2015)

- H. Mulaosmanovic, C. Monzio Compagnoni, N. Castellani, G. M. Paolucci, G. Carnevale, P. Fantini, D. Ventrice, A. L. Lacaita, A. S. Spinelli, A.Benvenuti: *Investigation of the turn-on of T-RAM cells under transient conditions.* IEEE Transactions on Electron Devices (ISSN:0018-9383), pp.1170-1176, 62 (2015)

- C. Monzio Compagnoni, G. M. Paolucci, C. Miccoli, A. S. Spinelli, A. L. Lacaita, A. Visconti, A. Goda: *First detection of single-electron charging of the floating gate of NAND Flash memory cells.* IEEE Electron Device Letters (ISSN:0741-3106), pp.132-134, 36 (2015)

- Y. Grachova, S. Vollebregt, A. L. Lacaita, P. M. Sarro: *High Quality Wafer-scale CVD Graphene on Molybdenum Thin Film for Sensing Application.* Procedia Engineering (ISSN:1877-7058), pp.1501-1504, 87 (2014)

- L. Crespi, A. Ghetti, M. Boniardi, A. L. Lacaita: *Electrical Conductivity Discontinuity at Melt in Phase Change Memory.* IEEE Electron Device Letters (ISSN:0741-3106) pp.747-749, 35 (2014)

- S. Brenna, A. Bonfanti, A. L. Lacaita: *A 6-fJ/conversion-step 200-kSps Asynchronous SAR ADC with Attenuation Capacitor in 130-nm CMOS adopting Standard MiM Capacitors.* Analog Integrated Circuits and Signal Processing (ISSN:0925-1030) pp.181-194, 9 (2014)

- H. Mulaosmanovic, G. M. Paolucci, C. Monzio Compagnoni, N. Castellani, G. Carnevale, P. Fantini, D. Ventrice, A. L. Lacaita, A. S. Spinelli, A. Benvenuti: *Working principles of a DRAM cell based on gated-thyristor bistability.* IEEE Electron Device Letters (ISSN:0741-3106) pp.921- 923, 35 (2014)

- G. M. Paolucci, C. Monzio Compagnoni, C. Miccoli, A. S. Spinelli, A. L. Lacaita, A. Visconti: *Revisiting charge trapping/detrapping in Flash memories from a discrete and statistical standpoint - Part II: on-field operation and distributed-cycling effects.* IEEE Trans. on. Electron Devices (ISSN:0018-9383) pp.2811- 2819, 61 (2014)

- G. M. Paolucci, C. Monzio Compagnoni, C. Miccoli, A. S. Spinelli, A. L. Lacaita, A. Visconti: *Revisiting charge trapping/detrapping in Flash memories from a discrete and statistical standpoint - Part I*: VT instabilities. IEEE Transactions on Electron Devices (ISSN:0018-9383) pp.2802-2810, 61 (2014)

- A.L. Lacaita, A. Redaelli: *The race of phase change memories to nanoscale storage and applications.* Microelectronic Engineering (ISSN:0167-9317) pp.351-356, 109 (2013)

- M. Boniardi, A. Redaelli, A. Ghetti, A.L. Lacaita: *Study of Cycling-Induced Parameter Variations in Phase Change Memory Cells.* IEEE Electron Device Letters (ISSN:0741-3106) pp.882-884, 34 (2013)

- G. Torrente, N. Castellani, A. Ghetti, C. Monzio Compagnoni, A. L. Lacaita, A. S. Spinelli, A. Benvenuti: *Investigation of the RTN amplitude statistics of nanoscale MOS devices by the statistical impedance field method.* Journal of computational Electronics (ISSN:1569-8025) pp. 585-591, 12 (2013)

- F. Pepe, A. Bonfanti, S. Levantino, C. Samori, A. L. Lacaita: *Suppression of Flicker Noise Up-Conversion in a 65-nm CMOS VCO in the 3.0-to-3.6 GHz Band.* IEEE Journal of Solid State Circuits (ISSN:0018-9200) pp. 2375-2389, 48 (2013)

- A. Ghetti, C. Monzio Compagnoni, A. Calloni, L. Vendrame, A. S. Spinelli, A. L. Lacaita: *Characterization and modeling of the band-to-band current variability of nanoscale device junctions.* IEEE Transactions on Electron Devices (ISSN:0018-9383) pp. 3291-3297, 60 (2013)

- S. Levantino, G. Marzin, C. Samori, A. L. Lacaita: *A Wideband Fractional-N PLL With Suppressed Charge-Pump Noise and Automatic Loop Filter Calibration.* IEEE Journal of Solid-State Circuits (ISSN:0018-9200) pp. 2419-2429, 48 (2013)

- A. Maconi, C. Monzio Compagnoni, A. S. Spinelli, A. L. Lacaita: *New erase constraint for the junction-less charge-trap memory array in cylindrical geometry.* IEEE Transactions on Electron Devices (ISSN:0018-9383) pp.2203-2208, 60 (2013)

- C. Miccoli, C. Monzio Compagnoni, L. Chiavarone, S. Beltrami, A. L. Lacaita, A. S. Spinelli, A. Visconti: *Reliability characterization issues for nanoscale Flash memories: a case study on 45-nm NOR devices.* IEEE Transactions on Device and Materials Reliability (ISSN:1530-4388), pp.362-369, 13 (2013)

- F. Pepe, A. Bonfanti, S. Levantino, C. Samori, A. L. Lacaita: *Analysis and Minimization of Flicker Noise Up-Conversion in Voltage-Biased Oscillators.* IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES (ISSN:0018-9480) pp. 2382-2394, 61 (2013)

- S. M. Amoroso, C. Monzio Compagnoni, A. Ghetti, L. Gerrer, A. S. Spinelli, A. L. Lacaita, A. Asenov: *Investigation of the RTN distribution of nanoscale MOS devices from subthreshold to on-state.* IEEE Electron Device Letters (ISSN:0741-3106), pp.683-685, 34 (2013)

- G. M. Paolucci, C. Monzio Compagnoni, N. Castellani, G. Carnevale, P. Fantini, D. Ventrice, A. L. Lacaita, A. S. Spinelli, A. Benvenuti: *Dynamic analysis of current-voltage characteristics of nanoscale gated-thyristors.* IEEE Electron Device Letters (ISSN:0741-3106) pp.629-631, 34 (2013)

- F. Adamu-Lema, C. Monzio Compagnoni, S. M. Amoroso, N. Castellani, L. Gerrer, S. Markov, A. S. Spinelli, A. L. Lacaita, A. Asenov: *Accuracy and issues of the spectroscopic analysis of RTN traps in nanoscale MOSFETs.* IEEE Transactions on Electron Devices (ISSN:0018-9383) pp.833-839, 60 (2013)

- A. Bonfanti , M. Ceravolo, G. Zambra, R. Gusmeroli, G. Baranauskas, G.N. Angotzi, A. Vato, E. Maggiolini, M. Semprini, A. Sottocornola Spinelli, A.L. Lacaita: *A Multi-Channel Low-Power System-on-Chip for in Vivo Recording and Wireless Transmission of Neural Spikes.* Journal of Low Power Electronics and Applications (ISSN:2079-9268) pp.211-241, 2 (2012)

- G. Marzin, S. Levantino, C. Samori, A. L. Lacaita: *A 20 Mb/s Phase Modulator Based on a 3.6 GHz Digital PLL With -36 dB EVM at 5 mW Power.* IEEE Journal of Solid-State Circuits (ISSN:0018-9200) pp.2974-2988, 47 (2012)

- C. Monzio Compagnoni, N. Castellani, A. Mauri, A. S. Spinelli, A. L. Lacaita: *Three-dimensional electrostatics- and atomistic doping-induced variability of RTN time constants in nanoscale MOS devices - Part II: spectroscopic implications.* IEEE Transactions on Electron Devices (ISSN:0018-9383) pp.2495-2500, 59 (2012)

- N. Castellani, C. Monzio Compagnoni, A. Mauri, A. S. Spinelli, A. L. Lacaita: *Three-dimensional electrostatics- and atomistic doping-induced variability of RTN time constants in nanoscale MOS devices - Part I: physical investigation.* IEEE Trans. on. Electron Devices (ISSN:0018-9383), pp.2488-2494, 59 (2012)

- G. M. Paolucci, C. Miccoli, C. Monzio Compagnoni, A. S. Spinelli, A. L. Lacaita: *String current in decananometer NAND Flash arrays: a compact-modeling investigation.* IEEE Transactions on Electron Devices (ISSN:0018-9383) pp.2331-2337, 59 (2012)

- S. Levantino, P. Maffezzoni, F. Pepe, A. Bonfanti, C. Samori, A. Lacaita: *Efficient Calculation of the Impulse Sensitivity Function in Oscillators.* IEEE Transactions on Circuits and Systems II, Express Briefs (ISSN:1549-7747) pp.628-632, 59 (2012)

- A. Bonfanti, F. Pepe, C. Samori, A. L. Lacaita: *Flicker Noise Up-Conversion due to Harmonic Distortion in Van der Pol CMOS Oscillators.* IEEE Transactions on Circuits and Systems I, Regular Papers (ISSN:1549-8328) pp.1418-1430, 7 (2012)

- A. S. Spinelli, C. Monzio Compagnoni, A. Maconi, S. M. Amoroso, A. L. Lacaita: *Quantum-mechanical charge distribution in cylindrical gate-all-around MOS devices.* IEEE Transactions on Electron Devices (ISSN:0018-9383) pp.1837-1843, 59 (2012)

- A. Maconi, A. Arreghini, C. Monzio Compagnoni, G. Van den Bosch, A. S. Spinelli, J. Van Houdt, A. L. Lacaita: *Comprehensive investigation of the impact of lateral charge migration on retention performance of planar and 3D SONOS devices.* Solid-State Electronics (ISSN:0038-1101) pp.64-70, 74 (2012);

- W. Wang, D. Loke, L. Shi, R. Zhao, H. Yang, L.-T. Law, L.-T. Ng, K.-G. Lim, Y.-C. Yeo, T.-C. Chong, A. L. Lacaita: *Enabling Universal Memory by Overcoming the Contradictory Speed and Stability Nature of Phase-Change Materials.* Scientific Reports (ISSN:2045-2322) pp.1-6, 2 (2012)

- M. Zanuso, S. Levantino, C. Samori, A. Lacaita: *A Glitch-Corrector Circuit for Low-Spur ADPLLs.* Analog Integrated Circuits and Signal Processing (ISSN:0925-1030) pp. 201-208, 73 (2012)

- D. Ielmini, A. L. Lacaita: *Phase change materials in non-volatile storage.* Materials Today (ISSN:1369-7021), pp.600-607, 14 (2011)

- M. Boniardi, D. Ielmini, I. Tortorelli, A. Redaelli, A. Pirovano, M. Allegra, M. Magistretti, C. Bresolin, D. Erbetta, A. Modelli, E. Varesi, F. Pellizzer, A. L. Lacaita, R. Bez: *Impact of Ge–Sb–Te compound engineering on the set operation performance in phase-change memories.* Solid-State Electronics (ISSN:0038-1101) pp.11-16, 58 (2011)

- Bonfanti, G. Zambra, G. Baranauskas, G. N. Angotzi, E. Maggiolini, M. Semprini, A. Vato, L. Fadiga, A. Sottocornola Spinelli, A. L. Lacaita: *A wireless microsystem with digital data compression for neural spike recording.* Microelectronic Engineering (ISSN:0167-9317) pp.1672-1675, 88 (2011)

- D. Tasca, M. Zanuso, G. Marzin, S. Levantino, C. Samori, A. L. Lacaita: *A 2.9–4.0-GHz Fractional-N Digital PLL With Bang-Bang Phase Detector and 560-fsrms Integrated Jitter at 4.5-mW Power.* IEEE Journal of Solid State Circuits (ISSN:0018-9200) pp.2745-2758, 46 (2011)

- S. M. Amoroso, C. Monzio Compagnoni, A. Mauri, A. Maconi, A. S. Spinelli, A. L. Lacaita: *Semi-analytical model for the transient operation of gate-all-around charge-trap memories.* IEEE Transactions on Electron Devices (ISSN:0018-9383) pp. 3116-3123, 58 (2011)

- A. Maconi, S. M. Amoroso, C. Monzio Compagnoni, A. Mauri, A. S. Spinelli, A. L. Lacaita: *Three-dimensional simulation of charge-trap memory programming - Part II: Variability.* IEEE Transactions on Electron Devices (ISSN:0018-9383) pp.1872-1878, 58 (2011)

- S. M. Amoroso, A. Maconi, A. Mauri, C. Monzio Compagnoni, A. S. Spinelli, A.L. Lacaita: *Three-dimensional simulation of charge-trap memory programming - Part I: Average behavior.* IEEE Transactions on Electron Devices (ISSN:0018-9383) pp.1864-1871, 58 (2011)

- D. Tasca, M. Zanuso, S. Levantino, C. Samori, A. L. Lacaita: *Low-Power Divider Retiming in a 3-4GHz Fractional-N PLL.* IEEE Transactions on Circuits and Systems II, Express Briefs (ISSN:1549-7747) pp.200-204, 58 (2011)

- M. Zanuso, S. Levantino, C. Samori, A. L. Lacaita: *A Wideband 3.6 GHz Digital Delta-Sigma Fractional-N PLL With Phase Interpolation Divider and Digital Spur Cancellation.* IEEE Journal of Solid-State Circuits (ISSN:0018-9200) pp.627-638, 46 (2011)

- D. Mantegazza, D. Ielmini, A. L. Lacaita: *Incomplete filament crystallization during set operation in PCM cells.* IEEE Electron Device Letters (ISSN:0741-3106) pp.341-343, 31 (2010)

- S. Lavizzari, D. Ielmini, A. L. Lacaita: *A new transient model for recovery and relaxation oscillations in phase change memories.* IEEE Transaction on Electron Devices (ISSN:0018-9383) pp.1838-1845, 57 (2010)

- M. Boniardi, D. Ielmini, S. Lavizzari, A. L. Lacaita, A. Redaelli, A. Pirovano: *Statistics of resistance drift due to structural relaxation in phase-change memory arrays.* IEEE Transactions on Electron Devices (ISSN:0018-9383) pp.2690-2696, 57 (2010)

- S. Lavizzari; D. Ielmini; A. L. Lacaita: *Transient simulation of delay and switching effects in phase change memories.* IEEE Transactions on Electron Devices (ISSN:0018-9383) pp.3257-3264, 57 (2010)

- D. Ielmini, F. Nardi, C. Cagli, A. L. Lacaita: *Size-dependent retention time in NiO-based resistive switching memories.* IEEE Electron Device Letters (ISSN:0741-3106) pp.353-355, 31 (2010)

- C. Monzio Compagnoni, C. Miccoli, A. L. Lacaita, A. Marmiroli, A. S. Spinelli, A. Visconti: *Impact of control-gate and floating-gate design on the electron-injection spread of decananometer NAND Flash memories.* IEEE Electronic Device Letters (ISSN:0741-3106) pp.1196-1198, 31 (2010)

- C. Monzio Compagnoni, L. Chiavarone, M. Calabrese, M. Ghidotti, A. L. Lacaita, A. S. Spinelli, A. Visconti: *Fundamental limitations to the width of the programmed VT distribution of NOR Flash memories.* IEEE Transactions on Electron Devices (ISSN:0018-9383) pp.1761-1767, 57 (2010)

- A. Mauri, C. Monzio Compagnoni, S. M. Amoroso, A. Maconi, A. Ghetti, A. S. Spinelli, A. L. Lacaita: *Comprehensive investigation of statistical effects in nitride memories - Part I: Physics-based modeling.* IEEE Transactions on Electron Devices (ISSN:0018-9383) pp.2116-2123, 57 (2010)

- C. Monzio Compagnoni, A. Mauri, S. M. Amoroso, A. Maconi, E. Greco, A. S. Spinelli, A. L. Lacaita: *Comprehensive investigation of statistical effects in nitride memories - Part II: Scaling analysis and impact on device performance.* IEEE Transactions on Electron Devices (ISSN:0018-9383) pp.2124-2131, 57 (2010)

- S. Levantino, L. Collamati, C. Samori, A. L. Lacaita: *Folding of Phase Noise Spectra in Charge-Pump Phase-Locked Loops Induced by Frequency Division.* IEEE Transactions on Circuits and Systems II, Express Briefs (ISSN:1549-7747) pp.671-675, 57 (2010)

- M. Zanuso, P. Madoglio, S. Levantino, C. Samori, A. L. Lacaita: *Time-to-Digital Converter for Frequency Synthesis based on a Digital Bang-Bang DLL.* IEEE Transactions on Circuits and Systems I, Regular Papers (ISSN:1549-8328) pp.548-555, 57 (2010)

- S. Levantino, M. Zanuso, P. Madoglio, D. Tasca, C. Samori, A. L. Lacaita: *AD-PLL for WiMAX with Digitally-Regulated TDC and Glitch Correction Logic.* Eurasip Journal on Embedded Systems (ISSN:1687-3955) pp.1-8, (2010)

Capitoli di Libri

- C. Monzio Compagnoni, A. S. Spinelli, A. L. Lacaita, A. Ghetti, A. Visconti: *Emerging constraints on NAND Flash memory reliability. in Nonvolatile Memories: Materials, Devices and Applications.* pp.267-293 (2012)

- Bonfanti, T. Borghi, G. Zambra, A. L. Lacaita: Fully Integrated Systems for Neural Signal Recording: *Technology Perspective and Low-Noise Front-End Design* in CMOS Biomicrosystem, Krzysztof Iniewski Ed. pp.33-73 (2011)

Contributi in Atti di Conferenze

- S. Brenna, P. Minotti, A. Bonfanti, G. Laghi, G. Langfelder, A. Longoni, A. L. Lacaita: *A Low-Noise Sub-500uW Lorentz Force Based Integrated Magnetic Field Sensing System.* In: IEEE MEMS 2015, pp. 932-935. Jan 18-22 2015, Estoril - Portugal (2015).

- M. Boniardi, A. Redaelli, C. Cupeta, F. Pellizzer, L. Crespi, G. D'Arrigo, A. L. Lacaita, G. Servalli: *Optimization Metrics for Phase Change Memory (PCM) Cell Architectures.* In: 2014 IEEE International Electron Devices Meeting. Dec.15-17 2014, San Francisco, CA USA (2014)

- G. M. Paolucci, M. Bertuccio, C. Monzio Compagnoni, S. Beltrami, A. S. Spinelli, A. L. Lacaita, A. Visconti: *Cycling-induced threshold-voltage instabilities in nanoscale NAND Flash memories: sensitivity to the array background pattern.* In: European Solid-State Device Research Conference (ESSDERC) pp.54-57. Sept.22-26 2014, Venezia, Italy (2014)

- H. Mulaosmanovic, C. Monzio Compagnoni, N. Castellani, G. Carnevale, D. Ventrice, P. Fantini, A. S. Spinelli, A. L. Lacaita, A. Benvenuti: *Data regeneration and disturb immunity of T-RAM cells.* In: European Solid-State Device Research Conference (ESSDERC) pp. 46-49. Venezia, Sept. 22-26, 2014, Italy (2014)

- S. Brenna, A. Bonfanti, A. Abba, F. Caponio, A. L. Lacaita: *Analysis and optimization of a SAR ADC with Attenuation Capacitor.* In: International Convention on Information and Communication Technology, Electronics and Microelectronics (MIPRO) pp. 68-73. May 26-30, 2014, Opatija, Croazia (2014)

- S. Brenna, A. Bonetti, A. Bonfanti, A. L. Lacaita: *A Simulation and Modeling Environment for the Analysis and Design of Charge Redistribution DACs used in SAR ADCs.* In: International Convention on Information and Communication Technology, Electronics and Microelectronics (MIPRO) pp. 74-79. May 26-30, 2014, Opatija, Croazia (2014)

- F. Pepe, A. Bonfanti, S. Levantino, A. L. Lacaita: *Impact of non-quasi-static effects on 1/f3 phase noise in a 1.9-to-2.6 GHz oscillator.* In: IEEE Radio Frequency Integrated Circuits Symposium, pp.425-428. June 1-3, 2014, Tampa, FL, USA (2014)

- G. M. Paolucci, C. Monzio Compagnoni, C. Miccoli, M. Bertuccio, S. Beltrami, J. Barber, J. Kessenich, A. L. Lacaita, A. S. Spinelli, A. Visconti: *A new spectral approach to modeling charge trapping/detrapping in NAND Flash memories.* In: International Reliability Physics Symposium, pp.2E.2.1-2E.2.6. June 01-05, 2014, Waikoloa, HI, USA (2014)

- H. Mulaosmanovic, G. M. Paolucci, C. Monzio Compagnoni, N. Castellani, G. Carnevale, P. Fantini, D. Ventrice, S. Viganò, A. M. Conti, N. Righetti, A. S. Spinelli, A. L. Lacaita, A. Benvenuti, A. Grossi: *Reliability investigation of T-RAM cells for DRAM applications.* In: International Reliability Physics Symposium, pp.MY.8.1- MY.8.4. June 01-05, 2014, Waikoloa, HI, USA (2014).

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- F. Pepe, A. Bonfanti, S. Levantino, P. Maffezzoni, C. Samori, A. L. Lacaita: *A simulation technique to compute phase noise induced from cyclostationary noise sources in RF oscillators.* In: Conference on VLSI Circuits and Systems VI. Apr. 24-26, 2013, Grenoble, France (2013)

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- M. Calabrese, C. Miccoli, C. Monzio Compagnoni, L. Chiavarone, S. Beltrami, A. Parisi, S. Bartolone, A. L. Lacaita, A. S. Spinelli, A. Visconti: *Accelerated reliability testing of Flash memory: accuracy and issues on a 45nm NOR technology.* In: International Conference on IC Design and Technology, pp.37-40. May 29-31, 2013, Pavia, Italy (2013).

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